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| 09/164,388 | 09/30/1998 | HON WAH CHIN | CISCPO54 | 6603 |

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| EXAMINER |
|---|
| PRIETO, BEATRIZ |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2142 | 16 |

DATE MAILED: 10/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/164,388 | Applicant(s) CHIN, HON WAH | |
|---|---|---|---|
| | Examiner B. PRIETO | Art Unit 2152 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

***Detailed Action***

1. This communication is in response to amendment filed 07/26/02, claims 1-54 remain pending.

2. Quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action may be found in previous office action.

3. Claims 1-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac et. al. (Calvignac) U.S. Patent No. 5,333,269 in view of Kurita et. al. (Kurita) U.S. Patent No. 5,920,568.

Regarding claims 1, 4, 10, 19, 20, 28, 37 Calvignac teaches substantial features of the invention as claimed, system/method of Figs. 1-2, 8 and 26, implemented on a interconnecting/routing node device (col 1/lines 45-49, col 3/lines 59-62); said device comprising;

a plurality of inbound and outbound controller interfaces (22) (2/lines 36-38), each comprising an inbound port (86-RCV) and an outbound port (86-XMIT), a memory (10), and a CPU (26) and inbound queue (LIQ) and outbound queue (LOQ);

each interface (22) comprising an inbound port (86-RCV) and an outbound port (86-XMIT), each said interface having a corresponding adapter (14) of a plurality of adapters through which the users are attached (Fig. 8);

receiving by each said interface (22) comprising inbound port (86-RCV) (col 2/line 1-6, 29-35, col 30/lines 3-17) an inbound message from attached users via each corresponding adapter (14) (86-receive circuit gets inbound data, 17/lines 49-62);

enqueues said message at selected inbound queue (LIQs) associated with said attached users (col 17/lines 63-67, col 8/lines 67-col 9/lines 12, said users having each an assigned inbound queue, col 27/lines 16-18, 29-31, 50-54);

determining when one of the plurality of inbound queues is ready to be moved to a corresponding destination outbound queue (col 12/lines 32-47, determining when to move, i.e.

dequeuing inbound queue) corresponding to the destination user to be transferred by the output port (86-xmit) to adapter (14) corresponding destination user (col 27/lines 16-18, 29-31, 50-54, destination port, col 29/lines 1-5, destination outbound queue col 28/lines 61-64);

transferring the inbound queue to the outbound queue associated with an outbound port (86-XMIT) (col 2/line 38-52, sending from inbound queue to outbound queue associated with a destination user, col 9/line 7-12), and enqueuing said transferred message at outbound queue corresponding to the destination user to be transferred by outbound port (86 XMIT) to said user (col 27/lines 19-28, providing to the adapter specific to the destination, outbound queue associated with outbound port (86 XMIT), col 23/lines 34-37) by the destination user;

receiving an instruction signal to handle an inbound queue, the inbound queue storing a plurality of packets (col 12/lines 32-47);

repeating the steps of receiving, providing, and storing until an instruction signal is asserted and received, initiating the said transfer step (Figs. 19A-B, 20-21);

storing a plurality of packets in one entry of an outbound queue (abstract: storing messages in buffer and chaining the buffers together generating inblund message queue and outbound message queue, col 1/line 60-col 2/line 6: received messages in data buffers, col 2/lines 14-19: outbound message queue is built by enqueueing the buffers onto said outbound message queue, col 2/lines 20-52: messages are received and enqueued in link inbound queue, an enqueue command causes the messages to be enqueued in an outbound queue, col 9/lines 7-18: data messages are enqueued in the link inbound queues and are sent to the link outbound queues);

however Calvignac teachings where inbound messages are queued in a selected inbound queue assigned to each user do not include classifying said messages in said selected inbound queue according to a sorting criteria;

Kurita teaches classifying the inbound packet in a selected one of the plurality of inbound queues (12) according to packet sorting criteria (11) (col 5/lines 47-50, 53-56) the selected inbound queue being associated with an outbound queue (col 5/lines 60-64);

It would have been obvious to one ordinary skilled in the art at the time the invention was made to modify Calvignac's system with means/apparatus for classifying the inbound packet in a selected one of the plurality of inbound queues according to packet sorting criteria; transferring one of plurality of inbound queue to one of the plurality of outbound queues

corresponding to the packet sorting criteria, as taught by Kurita, enabling means for repeating the steps of receiving, providing, classifying, and storing until an instruction signal is asserted and received, initiating the said transfer step, motivation would to provide a scheme suitable for use with routers and contrived to read data elements from a plurality of queues, scheme characterized in that the maximum value of time needed till the data elements are taken from within the queue does not depend on the number of data elements in other queues, where each queue treated impartially and the packets can be communicated without any decline in the throughput property.

Regarding claim 2, asserting an interrupt when it is determined that one of the plurality of inbound queues is ready to be moved to an outbound queue (Calvignac: col 12/lines 22-47) and transferring accordingly.

Regarding claim 3, classifying the inbound packet includes selecting inbound packet sorting criteria, obtaining packet sorting data (address) from inbound packet, said sorting data associated with a sorting criteria); and sorting the inbound packet into one of the plurality of inbound queues according to the packet sorting data (Kurita: col 5/lines 47-50, 53-56);

Regarding claim 5, storing by placing the inbound packet in the packet buffer from a pool of available buffers and storing the packet buffer in the inbound queue (Calvignac: col 2/lines 1-19, 29-35, Kurita: col 5/lines 44-64).

Regarding claim 6, determining whether a number of packets in one of the plurality of inbound queues exceeds a maximum number of packets (Calvignac: col 6/lines 22-25, col 7/lines 52-65, Fig. 11B, 13A).

Regarding claim 7, determining whether a number of bytes in one of the plurality of inbound queues exceeds a maximum number of bytes (Calvignac: Fig. 10A).

Regarding claim 8, determining whether a free pool of available memory has been depleted

(Calvignac: Fig. 16, (271), col 8/lines 14-41, determination means: col 15/lines 41-col 16/line 54).

Regarding claim 9, determining whether a maximum time limit has been exceeded (Calvignac: col 16/lines 30-36).

Regarding claim 11, receiving a notification from the controlling processor to handle the inbound queue (Calvignac: col 9/lines 7-19, col 12/lines 3-col 13/line 28).

Regarding claim 12, transmitting packets stored in the outbound queue (Calvignac: Fig. 23, functions performed by logic 506 and 508 for transmitting data packet bursts to the corresponding destination user).

Regarding claim 13, transmitting packets includes: selectively discarding packets stored in the outbound queue (Calvignac: col 7/lines 4-6, releasing means, col 14/lines 33-col 15/line 4).

Regarding claim 14, dequeing comprising, obtaining a next one of the plurality of inbound queues stored in the outbound queue; transmitting selected packets stored in the next one of the plurality of inbound queues; and releasing memory associated with the next one of the plurality of inbound queues (Calvignac: col 7/lines 4-6, releasing means, col 14/lines 33-col 15/line 4, Figs. 10A-B, (121)).

Regarding claim 15, storing the released memory in a free pool of available packet buffers (Calvignac: col 27/lines 36-61).

Regarding claim 16, forming a new inbound queue to be used by an inbound controller (Calvignac: col 14/lines 5-19).

Regarding claim 17, forming a queue to be used by the outbound controller during bi-directional

operation (Calvignac: Fig. 26).

Regarding claim 18, ascertaining a priority of the inbound queue based on a predetermined criteria; and transferring the inbound queue to the outbound queue according to the said priority of the inbound queue (Kurita: col 8/lines 62-67, col 9/line 1-col 10/line 53).

Regarding claim 21, providing the determined one of the plurality of inbound queues (Calvignac: enqueues at a selected inbound queue (LIQs) associated with said attached users, col 17/lines 63-67, col 8/lines 67-col 9/lines 12, said users having each an assigned inbound queue, col 27/lines 16-18, 29-31);

Regarding claim 22, a module adapted for asserting an interrupt when it is determined that one of the plurality of inbound queues is ready to be moved by the CPU to the outbound queue (Calvignac: interrupt: col 12/lines 22-37, col 9/lines 13-40: CPU 26 including order machine 90 performing data movement 86, said 86 control data transfer from inbound to outbound queue, col 9/lines 7-12, 36-42).

Regarding claim 23-27, this claim comprises the apparatus associated with the method disclosed on claim 5-9, respectively, same rationale is applicable.

Regarding claim 28, this claim comprises the apparatus associated with the method disclosed on claims (1, 4, 10, and 19-20), same rationale is applicable.

Regarding claim 29-36, this claim comprises the apparatus associated with the method disclosed on claims 11-18, respectively, same rationale is applicable.

Regarding claim 38, further selecting one of the plurality of inbound queues to be transferred to the outbound controller; (Calvignac: col 2/line 38-52, col 9/line 7-12), transfer associated with the packet sorting criteria (Kurita: col 5/lines 47-50, 53-56);

Regarding claim 39, designating memory for an inbound message to store said inbound packet based on classifying information (Kurita: col 5/lines 47-50, 53-56); releasing selected packet buffers associated with packets stored in the one of the plurality of outbound queues (Calvignac: Fig. 23, functions performed by logic 506 and 508 for transmitting data packet bursts to the destination) and selectively discarding packets stored in the outbound queue (Calvignac: col 7/lines 4-6, releasing means, col 14/lines 33-col 15/line 4).

Regarding claim 40, designating (obtaining) a next one of the plurality of inbound queues stored in the outbound queue; transmitting and releasing, as discuss above
(Calvignac: col 7/lines 4-6, releasing means, col 14/lines 33-col 15/line 4, Fig. 10A-B, (121)).

Regarding claim 41, a free pool of available packet buffers and the memory-releasing module is adapted for releasing the selected packet buffers into the free pool (Kurita: col 8/lines 62-6, col 1/lines 36-62, col 5/lines 44-56, col 8/lines 62-67, col 9/line 1-col 10/line 53).

Regarding claim 42, providing a new inbound queue to the inbound controller to replace the selected one of the plurality of inbound queues Calvignac: col 14/lines 5-19).

4. Claims 43-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac et. al. (Calvignac) U.S. Patent No. 5,333,269 in view of Kurita et. al. (Kurita) U.S. Patent No. 5,920,568 in further view of Gupta et. al. (Gupta) U.S. Patent No. 5,099,517.

Regarding claims 43, 49 and 50, including limitations discussed above on claims 1, 4, 10, 19, 20, 28, 37, however the combined teachings discussed above, do not teach encryption means wherein an encryption box coupled to the outbound controller, the encryption box being adapted for encrypting the inbound queue to provide an encrypted inbound queue to the outbound controller for transmission.

Gupta teaches cryptographic processing system/method (col 7/lines 62-65), wherein incoming data to be encrypted is stored in a packet buffer (14) and subsequently retrieved for cryptographic processing (16) and then forwarded to MAC processor (10) (col 8/lines 23-52);

processor 10 (i.e. MAC interface-outbound (output-transmit lines) controller 20) receives encrypted data for transmission (col 9/lines 33-41); encryption means (Figs. 2-3) require that complete blocks of data (e.g. multiples of eight bytes) be received by cryptographic module (26) from packet buffer for processing (col 15/lines 64-col 16/line 9); encryption of a packet buffer wherein data in a buffer is processed by encryption software (col 6/line 52-col 7/line 35).

It would have been obvious to one ordinary skilled in the art at the time the invention was made to modify existing system with encryption means wherein an encryption box coupled to the outbound controller, said encryption being adapted for encrypting the inbound queue to provide an encrypted inbound queue to the outbound controller for transmission, as taught by Gupta, motivation would be to enable the system to operate at network speeds on data streamed in real-time with out no additional packet buffers or additional processing capabilities.

Regarding claim 44, classifying the encrypted inbound queue in an outbound queue, the outbound controller adapted for transmitting data stored in the outbound queue (Kurita inbound/outbound controller for a router (Fig. 1 (11, 10), Fig. 6, (10), Fig. 7, (31, 38), Fig. 13 (50)), the router having an inbound port (Fig. 7 (31)) and an outbound port (Fig. 7 (38)), the inbound controller being adapted for receiving an inbound packet at the inbound port, the outbound controller being adapted for forwarding, for classifying the inbound packet in a selected one of the plurality of inbound queues according to packet sorting criteria (Kurita: Fig. 1, (11), Fig. 7, (33), col 1/lines 26-39, col 5/lines 44-56); means/apparatus for providing a plurality of inbound queues for the inbound port (Kurita: col 1/lines 35-62, col 5/lines 44-56, col 8/lines 62-67, col 9/line 1-col 10/line 53, Finkelstein: col 6/line 52-col 7/line 35).

Regarding claim 45-48, substantially the same or includes same limitation as claim 2, 22, 18, and 1, as discussed above, respectively, same rationale is applicable.

Regarding claim 52, outbound queue comprising entries identifying an inbound queue Inbound identifiers enqueued in outbound queue (col 28/lines 50-64).

Regarding claim 51, substantially the same limitation discussed on claims 22 and 2, same rationale is applicable.

Regarding claims 53-54, the computer-readable medium storing thereon computer-readable instructions and apparatus, respectively, for performing the method of claims 1, and 19, same rationale is applicable.

## *RESPONSE TO ARGUMENTS*

5. Applicant argues prior art of record (Calvignac) does not teach claim limitation as recited because Calvignac teaches according passage indicated by applicant, "identifying the address of the message to be enqueued", this is construed by applicant as a enqueing a single message and therefore distinguishable from claimed invention.

In response to applicant's argument, cited passage does not teach that an inbound queue stored a single message, nor it teaches that a message is equated to a packet. Claim limitation reads, storing a plurality of packets in an inbound queue; Prior art teaches storing a plurality of packets in one entry of an outbound queue (abstract: storing messages in buffer and chaining the buffers together generating inbound message queue and outbound message queue, col 1/line 60-col 2/line 6: received messages in data buffers, col 2/lines 14-19: outbound message queue is built by enqueueing the buffers onto said outbound message queue, col 2/lines 20-52: messages are received and enqueued in link inbound queue, an enqueue command causes the messages to be enqueued in an outbound queue, col 9/lines 7-18: data messages are enqueued in the link inbound queues and are sent to the link outbound queues); Arguments that prior teaches that a single message is a single packet, that it does not teach storing a plurality of messages in an inbound queue are not persuasive.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is

not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prieto, B. whose telephone number is (703) 305-0750. The Examiner can normally be reached on Monday-Friday from 6:00 to 3:30 p.m. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's Supervisor, Mark H. Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-6606. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800/4700.

Any response to this final action should be mailed to:

**Box AF**

**Commissioner of Patents and Trademarks**

**Washington, D.C. 20231**

**or Faxed to:**

(703) 746-7238 for TC 2100 Official After-final communications; please mark "EXPEDITED PROCEDURE", and

(703) 746-7239 for other TC 2100 Official communications.

**or:**

(703) 465-7240 for Non-Official, Draft communications, status query, please label "PROPOSED" or "DRAFT".

Or Telephone:

(703) 306-5631 for TC 2100 Customer Service Office

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

ROBERT B. HARRELL
PRIMARY EXAMINER

B. Prieto
GAU 2152
TC 2100
Patent Examiner
October 3, 2002